sml2008-am01: Decoded Instruction Format

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Abstract

This memo gives the decoded, 37-bit-wide, mostly-one-hot format used internally within the dock circuitry to represent an instruction.

Changes:	
21-Aug	Initial Revision
23-Oct	Changed polarity of bit 20 on "Shift" and "Set Data Latch"
	Noted that "Immediate→ILC" must have bit 7 set to 0
	Labeled bits 9 and 7 on last two instruction forms
29-Oct	Added TAIL instruction
	Removed "done" bit, relocated infinity bit
30-Oct	Divided move instruction into subinstructions based on path latch
31-Oct	Added encoding of Predicate field
01-Nov	Changed Rq to OS
	Changed Int to Int
	Swapped Z and !Z

Overview

FleetTwo Instructions in main memory occupy 37 bits. Of this, 11 bits give the path to the dock which is to execute the instruction; thus, only 26 of these bits are interpreted by the dock.

It is easiest to design the OD and EX stages of the dock if the control bits supplied there are mostly one-hot encoded. Moreover, due to layout considerations there is very little cost associated with making the instruction fifo 36 bits wide rather than 26 bits wide.

Due to these two considerations, all 26-bit instructions binary-coded-control instructions are expanded into 36-bit unary-coded-control instructions upon entry to the instruction fifo. This memo documents the 36-bit unary-coded-control format.

Predicate Field

The Predicate field, common to many instructions, consists of a six-bit wide, one-hot encoded field. The instruction will be **skipped** (not executed) if **any** condition corresponding to a bit whose value is one is met.

36 35 34 33 32 31 30 Z !Z !B B !A A

The Z flag is an "imaginary" flag which is "set" iff the outer loop counter is zero.

For example, if bits 31 and 34 are set, the instruction will be skipped if either the B flag is cleared or the A flag is set. Equivalently, it will be executed iff the B flag is set and the A flag is cleared.

Legend

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OS = One-Shot (0=Requeueing, 1=Not-Requeueing)
Int = Not Interruptible (0=Torpedoable, 1=Not-Torpedoable)
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Shift	Predicate	so	1 0 1 1 1	1	ļ	immediate	
Set Data Latch	Predicate	SO	26 27 26 24 23 23 1 0 1 1 1 1 1	0	10 17 14 14 14 14 14 14 14 14 14 14 14 14 14	immediate to	sign ext
	36 31	30 29	<u> </u>	21	16 15 14	Two	(+ c
Move, Immediate→Path	rredicate 31	38 29 29	27 26 25	21 20 19 18	16 15		מנפ
Move, DP[37:25]→Path	Predicate	70	1 1 0 1 1 27 26 25 24 23	Int	Do []		
Move, Path unchanged	Predicate	70	1 1 0 1 1	Int Ti	Do To		
Flush	Predicate	70	1 1 0 1 1	17			
	36 31	30 29	28 27 26 25 24 23 22		13 1	12	
Set Flags	Predicate	so	1 1 1 1 0			FlagA	FlagB
	36 31	30 29	28 27 26 25 24 23 22				
Decrement OLC	Predicate	0S	28 27 26 25 24 23 22	50			
Data Latch → OLC	Predicate	70	1 1 1 0				¢
$Immediate \rightarrow OLC$	Predicate	SO	1 1				Immediate
	36 31	30 29	28 27 26 25 24 23 22	50			
Data Latch → ILC	Predicate	S0	0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	1 8		α	ŭ
Immediate $ ightarrow \Pi$ C	Predicate	70	0 1 1 1 1 1			*0	Immediate
S → II.C	Redicate	30 29 OS	28 27 26 25 24 23 22 0 1 1 1 1 1 1 1			ω *	
				21			
Ē				•			

 \star – bit 8 is the "infinity" bit