sml2008-am01: Decoded Instruction Format

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Abstract

This memo gives the decoded, 37-bit-wide, mostly-one-hot format used internally within the dock circuitry to represent an instruction.

Changes:

Changes:	
14-Nov	Inverted bits 14 and 13 in the move instruction forms
10-Nov	Swapped order of FlagA and FlagB fields
	Documented Set Flags truth table field
01-Nov	Changed Rq to OS
	Changed Int to Int
	Swapped Z and !Z
31-Oct	Added encoding of Predicate field
30-Oct	Divided move instruction into subinstructions based on path latch
29-Oct	Added TAIL instruction
	Removed "done" bit, relocated infinity bit
23-Oct	Changed polarity of bit 20 on "Shift" and "Set Data Latch"
	Noted that "Immediate→ILC" must have bit 7 set to 0
	Labeled bits 9 and 7 on last two instruction forms
21-Aug	Initial Revision

Overview

FleetTwo Instructions in main memory occupy 37 bits. Of this, 11 bits give the path to the dock which is to execute the instruction; thus, only 26 of these bits are interpreted by the dock.

It is easiest to design the OD and EX stages of the dock if the control bits supplied there are mostly one-hot encoded. Moreover, due to layout considerations there is very little cost associated with making the instruction fifo 36 bits wide rather than 26 bits wide.

Due to these two considerations, all 26-bit instructions binary-coded-control instructions are expanded into 36-bit unary-coded-control instructions upon entry to the instruction fifo. This memo documents the 36-bit unary-coded-control format.

Predicate Field

The Predicate field, common to many instructions, consists of a six-bit wide, one-hot encoded field. The instruction will be **skipped** (not executed) if **any** condition corresponding to a bit whose value is one is met.

The Z flag is an "imaginary" flag which is "set" iff the outer loop counter is zero.

For example, if bits 31 and 34 are set, the instruction will be skipped if either the B flag is cleared or the A flag is set. Equivalently, it will be executed iff the B flag is set and the A flag is cleared.

Set Flags

Each of the FlagA and FlagB fields in the Set Flags instruction gives a truth table; the new value of the flag is the logical OR of the inputs whose bits are set to 1.

Legend

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OS = One-Shot (0=Requeueing, 1=Not-Requeueing)
Int = Not Interruptible (0=Torpedoable, 1=Not-Torpedoable)
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Shift	29 28 27 26 25 24 23 22 20 19 1 0 1 1 1 1 1 1 1	immediate
Set Data Latch	Predicate 0S 1 0 1 1 1 1 0 0 1 1 1 1 1 0 0 1 1 1 1	immediate to sign ext
Move, Immediate→Path	Predicate $\frac{31}{8}$ $\frac{30}{29}$ $\frac{28}{8}$ $\frac{27}{27}$ $\frac{26}{8}$ $\frac{27}{28}$	Immediate
Move, DP[37:25]→Path	29 28 27 26 25 24 23 22	
Move, Path unchanged Flush	Predicate 0S 0 1 1 0 1	
Set Flags	36 31 30 29 28 27 26 24 23 22 Predicate 0S 1 1 1 1 1 1 0	FlagB FlagA
Decrement OLC	36 Predicate OS 29 28 27 26 25 24 23 22 22 23 24 24 24 24	
Data Latch \rightarrow OLC Immediate \rightarrow OLC	31 30 29 26 27 26 26 24 23 22 22 0S 1 1 1 1 1 1 0 1	Immediate
Data Latch → ILC	36 Predicate 0S 0 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	ce cc
$\begin{array}{c} \text{Immediate} \rightarrow \text{ILC} \\ \\ \\ \\ \\ \\ \\ \\ \\ \\ \\ \\ \\ \\ \\ \\ \\ \\ \\$	Predicate 0S 20 20 1 <t< td=""><td></td></t<>	
TAIL	21	

 \star – bit 8 is the "infinity" bit \dagger – bit 28 is copied to the "flushing latch" whenever a move instruction occurs